Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 - 15. (Canceled)

16. (Currently Amended) A write clock present detector for a first-in first-out (FIFO) circuit, the write clock present detector comprising:

a read shift register having a first plurality of serially-coupled registers and configured to shift a read flag signal in response to a read clock;

a write shift register having a second plurality of serially-coupled registers and configured to shift a write flag signal in response to a write clock, wherein the first plurality of registers in the read shift register is larger in number compared to the second plurality of registers in the write shift register; and

a logic circuit coupled to an output of the read shift register and an output of the write shift register, and configured to logically combine the write flag signal with the read flag signal to generate a write clock present detect output signal.

17. (Canceled)

18. (Currently Amended) The write clock present detector of claim ~~17~~ 16 wherein the registers in the write shift register

and the registers in the read shift register are resettable registers with each having a reset input.

19. (Currently Amended) The write clock present detector of claim 18 ~~wherein the logic circuit comprises~~ comprising a reset circuit having an input coupled to an output of the read shift register, and an output coupled to the reset input of each of the registers in the read and the write shift registers.

20. (Original) The write clock present detector of claim 19 wherein the reset circuit comprises a serially-coupled pair of flip-flops coupled to an output of the read shift register and a logic gate having inputs coupled to outputs of the pair of flip-flops and an output coupled to the output of the reset circuit.

21. (Currently Amended) The write clock present detector claim ~~17~~ 16 wherein the write shift register comprises N registers and the read shift register comprises N+3 registers.

22. (Original) The write clock present detector of claim 21 wherein the logic circuit comprises:

a logic gate coupled to receive an output of the N^{th} write register and an output of the N^{th} read register and to generate a DET output signal; and

a flip-flop having a data input coupled to receive the DET output signal, a clock input coupled to the $(N+3)^{th}$ output of the read register, and an output coupled to generate a write clock present detect signal.

23. (Currently Amended) A method of detecting the presence of a write clock for a first-in first-out (FIFO) circuit, the method comprising:

propagating a read flag signal through a read shift register, comprising a first set of registers, in response to a read clock;

propagating a write flag signal through a write shift register, comprising a second set of registers wherein the second set of registers is smaller in number than the first set of registers, in response to the write clock; and

comparing an output of the read shift register with an output of the write shift register to generate a write clock present output signal.

24. (Original) The method of claim 23 further comprising periodically resetting the read shift register and the write shift register.

25 - 28. (Canceled)

29. (Previously Presented) The write clock present detector of claim 16 wherein the write clock present detect output signal is generated when the read and write flag signals propagate to the logic circuit.

30. (Currently Amended) ~~The write clock present detector of claim 16 comprising~~ A write clock present detector for a first-in first-out (FIFO) circuit, the write clock present detector comprising:

a read shift register having a first plurality of serially-coupled registers and configured to shift a read flag signal in response to a read clock;

a write shift register having a second plurality of serially-coupled registers and configured to shift a write flag signal in response to a write clock;

another shift register coupled to receive the output of the read shift register to generate a delayed read flag signal; and

a logic circuit coupled to an output of the read shift register and an output of the write shift register, and configured to logically combine the write flag signal with the read flag signal to generate a write clock present detect output signal, wherein the logic circuit comprises:

a logic gate coupled to receive the output of the write shift register and the output of the read shift register; and

a register having a data input coupled to receive an output of the logic gate and having a clock input coupled to receive the delayed read flag signal to generate a write clock present signal.

31. (Previously Presented) The method of claim 23 wherein the write clock present output signal is generated when the read and write flag signals propagate to a logic circuit.

32. (Previously Presented) The method of claim 23 wherein the write clock present output signal is generated when the read and write flag signals propagate to a logic circuit before a reset occurs.

33. (Previously Presented) The method of claim 23 comprising delaying the generation of the write clock present output signal after comparing the output of the read and write shift registers.

34. (Previously Presented) The method of claim 23 comprising further propagating the read flag signal through the read shift register in response to the read clock to generate the write clock present output signal.

35. (Previously Presented) The method of claim 23 comprising clocking a register with the further propagated read flag signal to generate the write clock present output signal.

36. (Currently Amended) ~~The method of claim 23 comprising~~ A method of detecting the presence of a write clock for a first-in first-out (FIFO) circuit, the method comprising:

propagating a read flag signal through a read shift register in response to a read clock;

propagating a write flag signal through a write shift register in response to the write clock;

comparing an output of the read shift register with an output of the write shift register to generate a write clock present output signal; and

using the read flag signal to generate a reset signal for the read and write shift registers.

37. (Currently Amended) The method of claim ~~23 comprising~~ 36 wherein using comprises further propagating the read flag signal through the read shift register in response to the read clock to generate [[a]] the reset signal for the read and write shift registers.

38. (Previously Presented) The method of claim 23 comprising initiating the propagation of the read flag signal and the write flag signal after generation of a reset signal for the read and write shift registers.

39. (New) The write clock present detector of claim 16 wherein the read shift register generates a delayed read flag signal and wherein the logic circuit comprises:

a logic gate coupled to receive the output of the write shift register and the output of the read shift register; and

a register having a data input coupled to receive an output of the logic gate and having a clock input coupled to receive the delayed read flag signal to generate a write clock present signal.

40. (New) The method of claim 23 comprising using the read flag signal to generate a reset signal for the read and write shift registers.

41. (New) The method of claim 23 comprising further propagating the read flag signal through the read shift register in response to the read clock to generate a reset signal for the read and write shift registers.